Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A memory device comprising:

a plurality of memory units each corresponding to an address for recording data;

an interface circuit for receiving address information;

an address calculation module connected to the interface circuit for providing a first address according to the address information;

an address buffer connected to the address calculation module for receiving and storing addresses provided by the address calculation module, wherein the address calculation module is capable of generating and providing a second address different from the first address according to the address information after the address buffer stores the first address; and

a decoding module connected to the address buffer for enabling each memory unit corresponding to the first address to output its data when the address buffer stores the first address, the address calculation module capable of providing the second address after each memory unit corresponding to the first address outputs its data, the address buffer being capable of storing the

second address provided by the address calculation module, and the decoding module being capable of enabling each memory unit corresponding to the second address to output its data.

[c2] 2.The memory device of claim 1 wherein at least two of the plurality of memory units are corresponding to the same address, and the memory device further comprises: at least one output buffer each connected to each memory unit corresponding to the same address, when each memory unit corresponding to the same address synchronously outputs its data, the output buffer is capable of storing the output data provided by each memory unit and providing data as output of the memory device for each memory unit at different times in turn.

[c3] 3.The memory device of claim 2 wherein the output buffer comprises:

a first and second latch circuit each respectively connected to different memory units corresponding to the same address for storing the data provided by each memory unit, the output buffer setting the data stored in the first latch circuit as the output of the memory device; and

a transmission circuit connected to the two latch circuits, when the memory units connected to the first latch circuit and the second latch circuit output data, the trans-

mission circuit shuts down and enables the first and the second latch circuits to be capable of respectively storing data provided by two memory units; and when data stored in the first latch circuit was set for the output of the memory device by the output buffer, the transmission circuit turns on and transmits data stored in the second latch circuit to the first latch circuit and enables the output module to be capable of setting the data stored in the first latch circuit for the output of the memory device so that the output buffer is capable of providing data outputted from each memory unit at different times in turn.

[c4] 4.The memory device of claim 3 wherein the transmission circuit is a transmission gate.

[c5] 5.The memory device of claim 2 wherein the output buffer is further connected to the interface circuit and provides output data for each memory unit in turn through the bus of the interface circuit set for receiving the address information.

[c6] 6.The memory device of claim 1 wherein the memory device is a non-volatile memory.

[c7] 7.The memory device of claim 1 wherein the address calculation module calculates the second address by

progressively increasing addresses from the first address.

[c8] 8.The memory device of claim 1 wherein the plurality of memory units are arrayed in a matrix, and the decoding module comprises a column decoder and a row decoder.

[c9] 9.A memory device comprising:
a plurality of memory units each corresponding to an address for recording data, wherein at least two memory units are corresponding to the same address;
a decoding module capable of receiving an address and enabling each memory unit corresponding to the address to output its data; and
at least one output buffer each connected to memory units corresponding to the same address, when the memory units corresponding to the same address output their data synchronously, the output buffer is capable of storing data provided by each memory unit and at different times providing data provided by each memory unit in turn for being output of the memory device.

[c10] 10.The memory device of claim 9 wherein the output buffer comprises:
a first and second latch circuit each respectively connected to different memory units corresponding to the same address for storing the data provided by each

memory unit, the output buffer setting the data stored in the first latch circuit as the output of the memory device; and

a transmission circuit connected to the two latch circuits, when the memory units connected to the first latch circuit and the second latch circuit output data, the transmission circuit shuts down and enables the first and the second latch circuits to be capable of respectively storing data provided by two memory units; and when data stored in the first latch circuit was set for the output of the memory device by the output buffer, the transmission circuit turns on and transmits data stored in the second latch circuit to the first latch circuit and enables the output module to be capable of setting the data stored in the first latch circuit for the output of the memory device so that the output buffer is capable of providing data outputted from each memory unit at different times in turn.

[c11] 11.The memory device of claim 10 wherein the transmission circuit is a transmission gate.

[c12] 12.The device of claim 9 comprises:

an interface circuit for receiving address information;

an address calculation module for providing a first address according to the address information;

an address buffer connected to the address calculation

module for receiving and storing the first address provided by the address calculation module, wherein the address calculation module is capable of generating and providing a second address different from the first address according to the address information after the address buffer stores the first address; and
wherein the decoding module is connected to the address buffer for enabling each memory unit corresponding to the first address to output its data when the address buffer stores the first address, the address calculation module capable of providing the second address after each memory unit corresponding to the first address outputs its data, the address buffer being capable of storing the second address provided by the address calculation module, and the decoding module being capable of enabling each memory unit corresponding to the second address to output its data.

[c13] 13.The memory device of claim 12 wherein the output buffer is further connected to the interface circuit and provides output data for each memory unit in turn through the bus of the interface circuit set for receiving the address information.

[c14] 14.The memory device of claim 11 wherein the address calculation module calculates the second address by progressively increasing addresses from the first ad-

dress.

[c15] 15.The memory device of claim 9 wherein the memory device is a non-volatile memory.

[c16] 16.The memory device of claim 9 wherein the plurality of memory units are arrayed in a matrix, and the decoding module comprises a column decoder and a row decoder.